DDR3L-1600 ECC SO-DIMM Module

8GB 2-Rank

Based on 4Gbit (512Mx8) component

Revision 1.0 (January, 2013)
-Initial Release

1.0 Feature

- V_{DD} = 1.35V (1.283V – 1.45V)
- Backward compatible to V_{DD} = 1.5V (1.425V – 1.575V)
- Programmable CAS Latency: 5, 6, 7, 8, 9, 10, 11
- Programmable Additive Latency(Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066), 7(DDR3-1333) and 8(DDR3-1600)
- 400MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with t_{CCD} = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Internal (self) calibration: Internal self-calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- Bi-directional Differential Data Strobe
- Asynchronous Reset
- On-Die termination using ODT pin
- 8 independent internal bank
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
- Serial presence detect with EEPROM
- Dimensions (Nominal) 30.0 mm high, 67.75 mm wide
- Based on JEDEC standard reference Raw Cards Lay out.
- Halogen-free and RoHS compliant
- Gold plated contacts

2.0 Ordering Information

Part number	Density	Module Organization	Component composition	Component PKG	Module Rank	Description
W16ESB8GLH	8GB	1Gx72	512Mx8 x18pcs	FBGA	2	PC3-12800

Note: Last Character of the Part Number (x) representing DRAM vendor
S=Samsung; M=Micron; H=Hynix

3.0 Key Timing Parameters

	DDR3L-1600	Unit
CL-tRCD-tRP	11-11-11	tCK
CAS Latency	11	tCK
tCK(min)	1.25	ns
tRCD(min)	13.5	ns
tRP(min)	13.5	ns
tRAS(min)	35	ns
tRC(min)	48.75	ns

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
V_{in} , Vout	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V
V_{DD}	Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	-0.4 ~ 1.975	V
V_{DDQ}	Short circuit current	-0.4 ~ 1.975	V
V_{DDL}	Power dissipation	-0.4 ~ 1.975	V
T_{STG}	Storage Temperature	-55 ~ + 100	°C

5.0 DIMM Pin Configurations (Front side/Back side)

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	V_{SS}	105	A1	157	DM5	2	V_{SS}	54	DQ28	106	A2	158	V_{SS}
3	V_{SS}	55	DQ24	107	A0	159	DQ42	4	DQ4	56	DQ29	108	BA1	160	DQ46
5	DQ0	57	DQ25	109	V_{DD}	161	DQ43	6	DQ5	58	V_{SS}	110	V_{DD}	162	DQ47
7	DQ1	59	DM3	111	CK0	163	V_{SS}	8	V_{SS}	60	DQS3#	112	CK1	164	V_{SS}
9	V_{SS}	61	V_{SS}	113	CK0#	165	DQ48	10	DQS0#	62	DQS3	114	CK1#	166	DQ52
11	DM0	63	DQ26	115	V_{DD}	167	DQ49	12	DQS0	64	V_{SS}	116	V_{DD}	168	DQ53
13	DQ2	65	DQ27	117	A10/AP	169	V_{SS}	14	V_{SS}	66	DQ30	118	NC	170	V_{SS}
15	DQ3	67	V_{SS}	119	BA0	171	DQS6#	16	DQ6	68	DQ31	120	NC	172	DM6
17	V_{SS}	69	CB0	121	WE#	173	DQS6	18	DQ7	70	V_{SS}	122	RAS#	174	DQ54
19	DQ8	71	CB1	123	V_{DD}	175	V_{SS}	20	V_{SS}	72	CB4	124	V_{DD}	176	DQ55
21	DQ9	73	V_{SS}	125	CAS#	177	DQ50	22	DQ12	74	CB5	126	ODT0	178	V_{SS}
23	V_{SS}	75	DQS8#	127	S0#	179	DQ51	24	DQ13	76	DM8	128	ODT1	180	DQ60
25	DQS1#	77	DQS8	129	S1#	181	V_{SS}	26	V_{SS}	78	V_{SS}	130	A13	182	DQ61
27	DQS1	79	V_{SS}	131	V_{DD}	183	DQ56	28	DM1	80	CB6	132	V_{DD}	184	V_{SS}
29	V_{SS}	81	CB2	133	DQ32	185	DQ57	30	RESET#	82	CB7	134	DQ36	186	DQS7#
31	DQ10	83	CB3	135	DQ33	187	V_{SS}	32	V_{SS}	84	V_{REFCA}	136	DQ37	188	DQS7
33	DQ11	85	V_{DD}	137	V_{SS}	189	DM7	34	DQ14	86	V_{DD}	138	V_{SS}	190	V_{SS}
35	V_{SS}	87	CKE0	139	DQS4#	191	DQ58	36	DQ15	88	NF/A15[1]	140	DM4	192	DQ62
37	DQ16	89	CKE1	141	DQS4	193	DQ59	38	V_{SS}	90	NF/A14[2]	142	DQ38	194	DQ63
39	DQ17	91	BA2	143	V_{SS}	195	V_{SS}	40	DQ20	92	A9	144	DQ39	196	V_{SS}
41	V_{SS}	93	V_{DD}	145	DQ34	197	SA0	42	DQ21	94	V_{DD}	146	V_{SS}	198	EVENT#
43	DQS2#	95	A12	147	DQ35	199	V_{DDSPD}	44	DM2	96	A11	148	DQ44	200	SDA
45	DQS2	97	A8	149	V_{SS}	201	SA1	46	V_{SS}	98	A7	150	DQ45	202	SCL
47	V_{SS}	99	A5	151	DQ40	203	V_{TT}	48	DQ22	100	A6	152	V_{SS}	204	V_{TT}
49	DQ18	101	V_{DD}	153	DQ41	–	–	50	DQ23	102	V_{DD}	154	DQS5#	–	–
51	DQ19	103	A3	155	V_{SS}	–	–	52	V_{SS}	104	A4	156	DQS5	–	–

Notes: 1. Pin 88 is NF for 2GB and 4GB; A14 for 8GB.
2. Pin 90 is NF for 1GB; A14 for 4GB and 8GB.

6.0 DIMM Pin Description

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

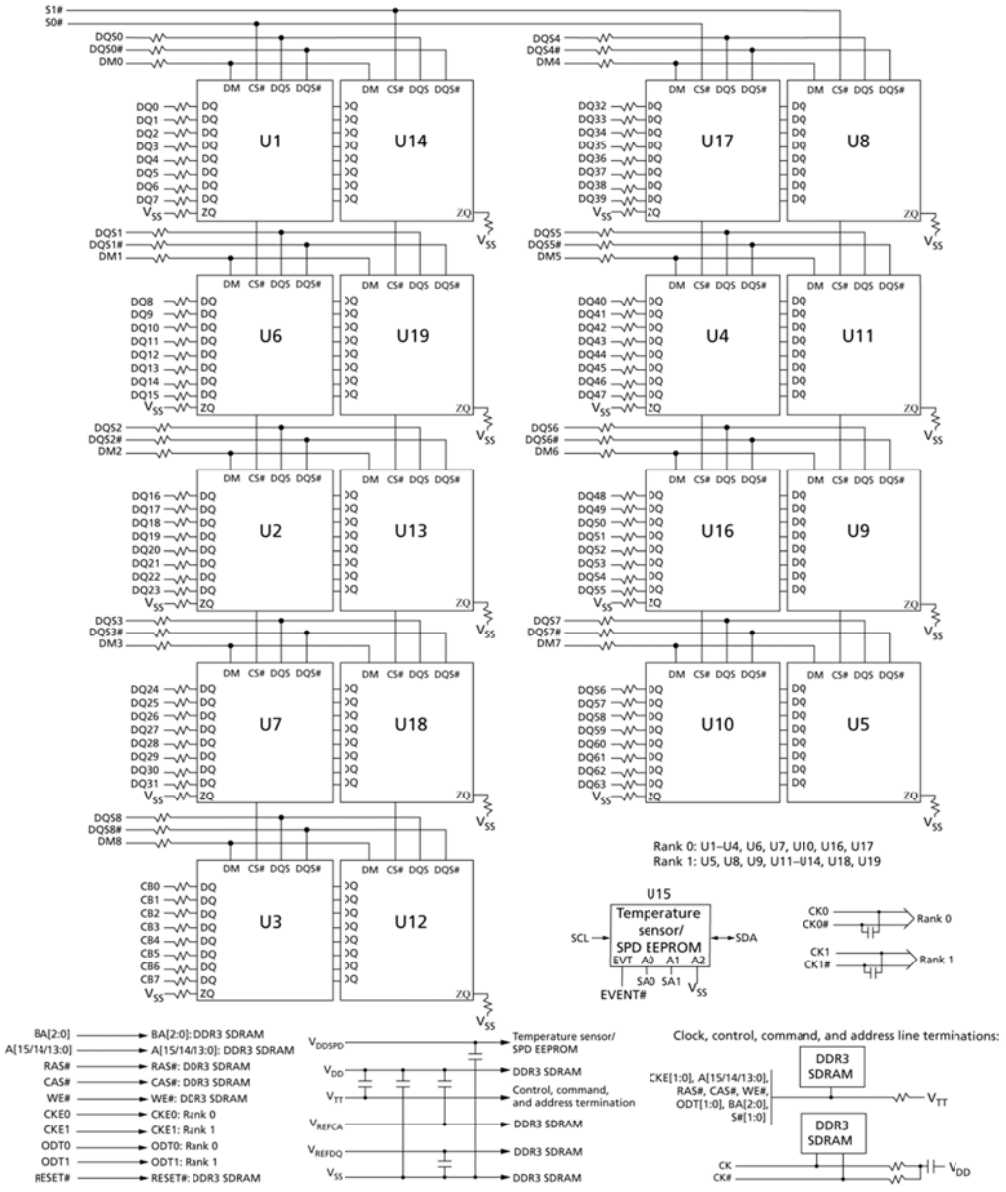
Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

7.0 Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Pre-charge
512Mx8(4Gb)base	A0-A15	A0-A9	BA0-BA2	A10

8.0 Functional Block Diagram: 8GB; 1Gx72 Module (Populated as 2 ranks of x8 SDRAM Module)



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

9.0 AC & DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.425	1.5	1.575	V
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V
$V_{REF}DQ_{(DC)}$	I/O Reference Voltage (DQ)	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V
$V_{REF}CA_{(DC)}$	I/O Reference Voltage (CMD/Add)	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V
V_{TT}	Termination Voltage	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	V

10.0 Capacitance (Max.)

Symbol	Parameter/Condition	Min	Max	Unit
CCK	Input capacitance, CK and $\overline{CK}$	-	11	pF
CI1	Input capacitance, CKE and $\overline{CS}$	-	12	pF
CI2	Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-	12	pF
CIO	Input capacitance, DQ, DM, DQS, $\overline{DQS}$	-	10	pF

11.1 AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Parameter	Symbol	DDR3L-1600		Units
		min	max	
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	ns
Average Clock Period	tCK(avg)	-		
Clock Period	tCK(abs)	tCK(avg) min +tJIT (per)min	tCK(avg) max +tJIT (per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-70	70	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	ps
Cycle to Cycle Period Jitter	tJIT(cc)	140	-	ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120	-	ps
Cumulative error across 2 cycles	tERR(2per)	- 103	103	ps
Cumulative error across 3 cycles	tERR(3per)	- 122	122	ps
Cumulative error across 4 cycles	tERR(4per)	- 136	136	ps
Cumulative error across 5 cycles	tERR(5per)	- 147	147	ps
Cumulative error across 6 cycles	tERR(6per)	- 155	155	ps
Cumulative error across 7 cycles	tERR(7per)	- 163	163	ps
Cumulative error across 8 cycles	tERR(8per)	- 169	169	ps
Cumulative error across 9 cycles	tERR(9per)	- 175	175	ps
Cumulative error across 10 cycles	tERR(10per)	- 180	180	ps

11.2 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3L-1600		Units
		min	max	
Cumulative error across 11 cycles	tERR(11per)	- 184	184	ps
Cumulative error across 12 cycles	tERR(12per)	- 188	188	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max		ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	tCK(avg)
Data Timing				
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK(avg)
DQ low-impedance time from CK, /CK	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	225	ps
Data setup time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDS(base) AC175	TBD	-	ps
	tDS(base) AC150	10	-	ps
Data hold time to DQS, /DQS referenced to Vih(ac)Vil(ac) levels	tDH(base) DC100	45	-	ps
DQ and DM Input pulse width for each input	tDIPW	360	-	ps
Data Strobe Timing				
DQS, /DQS READ Preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential READ Postamble	tRPST	0.3	-	tCK
DQS, /DQS output high time	tQSH	0.4	-	tCK(avg)
DQS, /DQS output low time	tQSL	0.4	-	tCK(avg)
DQS, /DQS WRITE Preamble	tWPRE	0.9	-	tCK
DQS, /DQS WRITE Postamble	tWPST	0.3	-	tCK
DQS, /DQS rising edge output access time from rising CK, /CK	tDQSCK	-225	225	ps
DQS, /DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	ps
DQS, /DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	0.27	tCK(avg)
DQS,DQS faling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK(avg)
DQS,DQS faling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK(avg)
DLL locking time	tDLLK	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))		nCK

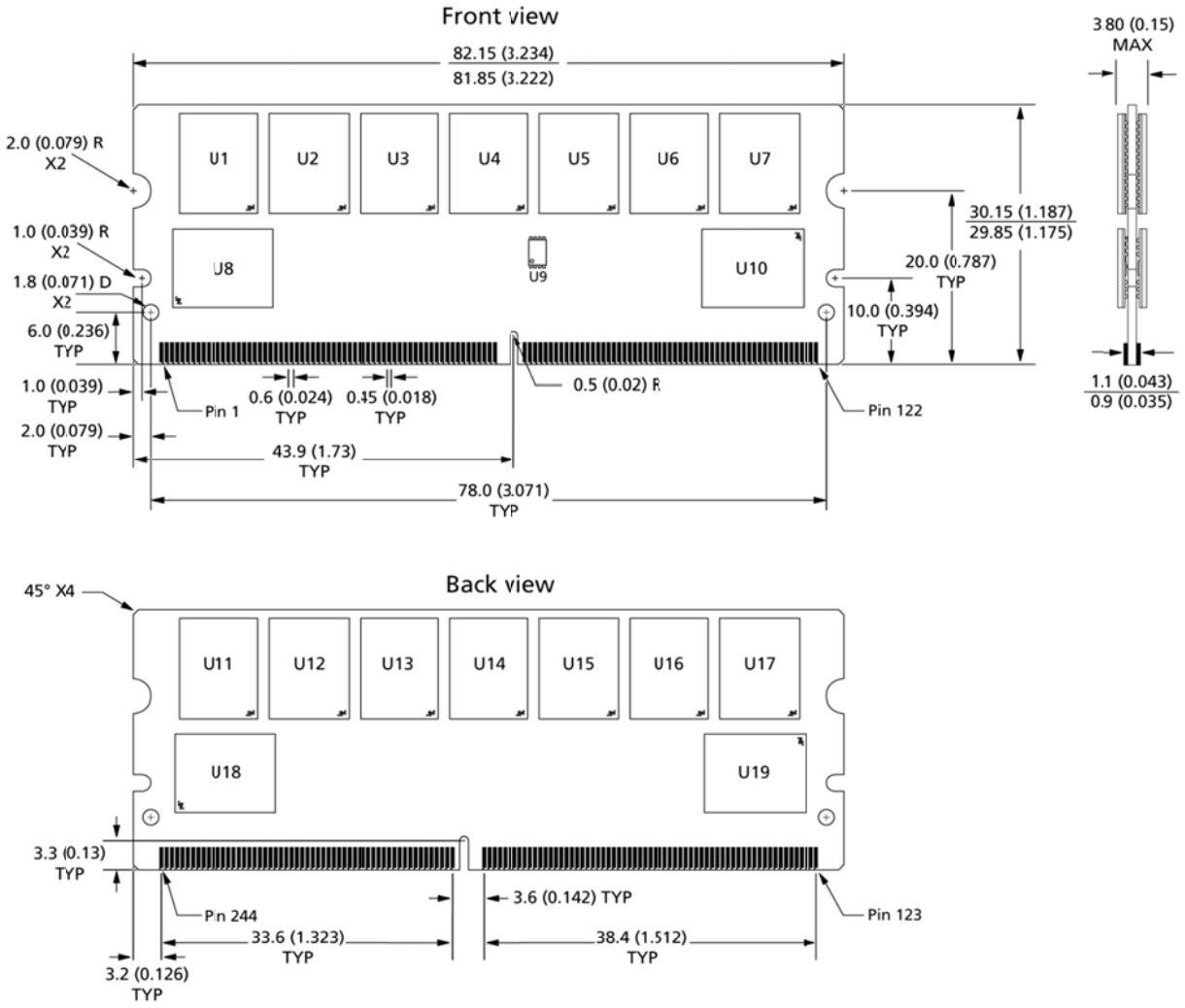
11.3 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3L-1600		Units
		min	max	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	ns
Four activate window for 2KB page size	tFAW	40	-	ns
Command and Address setup time to CK, /CK referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC175	45	-	ps
	tIS(base) AC150	45+125	-	ps
Command and Address hold time from CK, /CK referenced to Vih(ac) / Vil(ac) levels	tIH(base) DC100	120	-	ps
Control & Address Input pulse width for each input	tIPW	560	-	ps
Calibration Timing				
Power-up and RESET calibration time	tZQinitI	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	tCK
Reset Timing				
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC+ 10ns)	-	
Self Refresh Timing				
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC+ 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10tCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3tCK, 5 ns)	-	
Command pass disable delay	tCPDED	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	nCK

11.4 AC Timing Parameters & Specifications (cont.)

Parameter	Symbol	DDR3L-1600		Units
		min	max	
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
ODT Timing				
ODT high time without write command or with wirte commandand BC4	ODTH4	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	tCK
Setup time for tDQSS latch	tWLS	165	-	ps
Hold time of tDQSS latch	tWLH	165	-	ps
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

12.0 Physical Dimensions: 1Gx72 (2 Ranks) (512Mx8 Based)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.